UNIVERSITÉ PARIS-SACLAY · MASTER 1 SAIETI · PAPER STUDY, 2026

A 6.5 kV SiC MOSFET Full-Bridge Power Module

A technical study of Boutry, Rogers, Lemmon, Turner and Baker (IWIPP 2025): design, fabrication, characterization, and the questions the paper leaves open

Summary. The paper presents what the authors describe as the first full-bridge SiC MOSFET module above 1.7 kV: four 6.5 kV GeneSiC dies in an XHP3 footprint, built first as a sub-scale prototype on FR4 with an ABS housing. The prototype shows a simulated commutation inductance of 34.5 nH (target 20 nH), an on-resistance of about 300 mΩ that matches the datasheet, leakage measured to 3.0 kV, and double-pulse switching at 2.5 kV and 10 A with less than 200 V of turn-off overshoot but strong current ringing. This report explains each step in my own words and diagrams, then adds my own analysis. A back-of-envelope check shows the turn-off di/dt must have stayed below about 5.8 A/ns. The eutectic solder runs at 98 % of its absolute melting temperature at the die's 175 °C rating. Simple loss and derating numbers are given for the full-scale target. A simulation plan, which I intend to carry out, would quantify the ringing and the benefit of reaching 20 nH.

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Paper A. Boutry, M. Rogers, A. N. Lemmon, N. Turner, N. Baker, "A 6.5 kV Full-Bridge SiC MOSFET Module Design," 2025 IEEE International Workshop on Integrated Power Packaging (IWIPP), The University of Alabama. DOI: 10.1109/IWIPP61784.2025.10971507

Nature A study of published work, not hardware I built. All figures here are my own drawings. The paper's photographs and measured plots are not reproduced; readers should consult the paper. Sections marked MY ANALYSIS go beyond the paper.

Origin Written up from my M1 oral presentation (October 2026)

1 · Why medium-voltage SiC modules matter

Three applications are pushing power electronics to higher voltage: megawatt charging for heavy electric vehicles, rail traction at 3.3 kV and above, and solid-state transformers that connect converters directly to the medium-voltage grid. In each case, a higher operating voltage means lower current for the same power, so thinner conductors, smaller magnetics and higher power density.

Silicon carbide makes this possible. Its bandgap (about 3.3 eV against 1.1 eV for silicon) gives roughly ten times the critical electric field, so a SiC MOSFET blocks a given voltage with a much thinner, lower-resistance drift layer. It also switches faster and tolerates higher junction temperature. A bare die is not a usable product, though: it has to be connected, cooled, insulated and protected by a package. According to the paper, packaged SiC modules are widely available at 1.2–1.7 kV and a few at 3.3 kV, while 6.5 kV modules have been announced but not released.

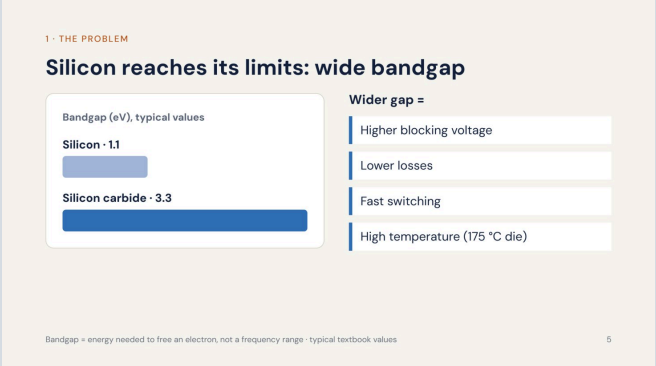


Figure 1. Bandgap comparison and what a wider gap buys (own slide, typical textbook values).

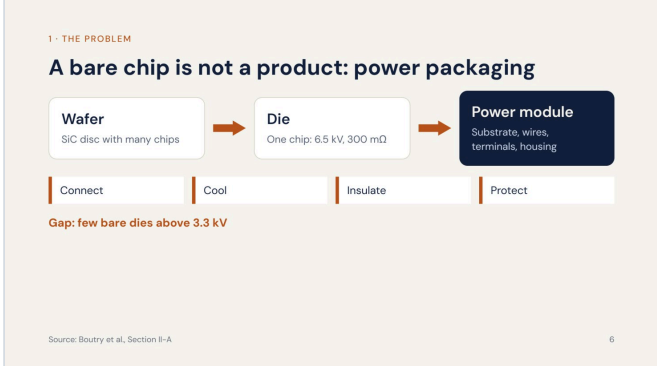


Figure 2. From wafer to die to module: packaging is what makes a die usable (own slide).

2 · What the paper proposes

Almost all SiC modules today are half bridges, so a full-bridge converter needs two modules and a three-phase inverter needs three. Earlier full-bridge SiC modules exist at 1.2 kV and 1.7 kV (Kell, Knoll, Rajagopal et al.), and a 3.3 kV full-bridge building block has been made from two half-bridge modules (Ismail et al.). The authors found no full-bridge module above 1.7 kV. Their contribution is a **6.5 kV full-bridge module** in the industry-standard **XHP3** footprint (100 × 140 mm), aimed at transformer-isolated dc-dc converters with a medium-voltage input.

The XHP3 has a dual-tab phase terminal, which suits a full bridge. The module uses two identical half-bridge substrates, which keeps the design simple and the two legs symmetric. Linking the AC1 and AC2 terminals turns the full bridge into a half bridge with twice the current capability, so one product serves both topologies.

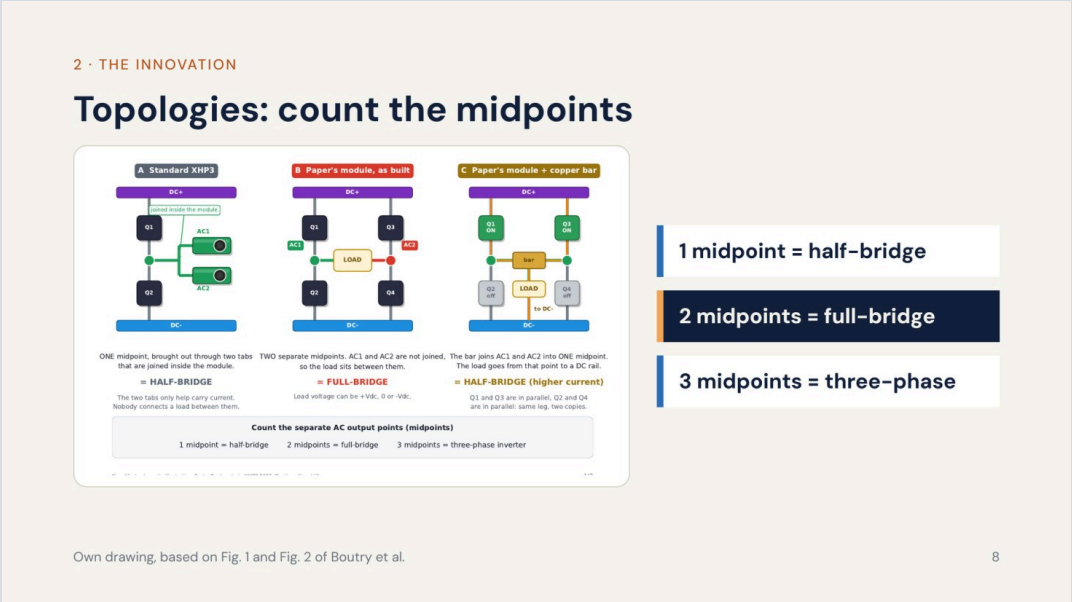


Figure 3. Half bridge, full bridge and three-phase: count the midpoints (own drawing based on the paper's schematic and layout).

The selected die is the GeneSiC **G2R300MT6-CAL**: 6.5 kV, 300 mΩ, maximum junction temperature 175 °C, one of very few bare dies commercially available above 3.3 kV. The authors had characterized it before in a simple test package (Baker et al., PCIM 2023).

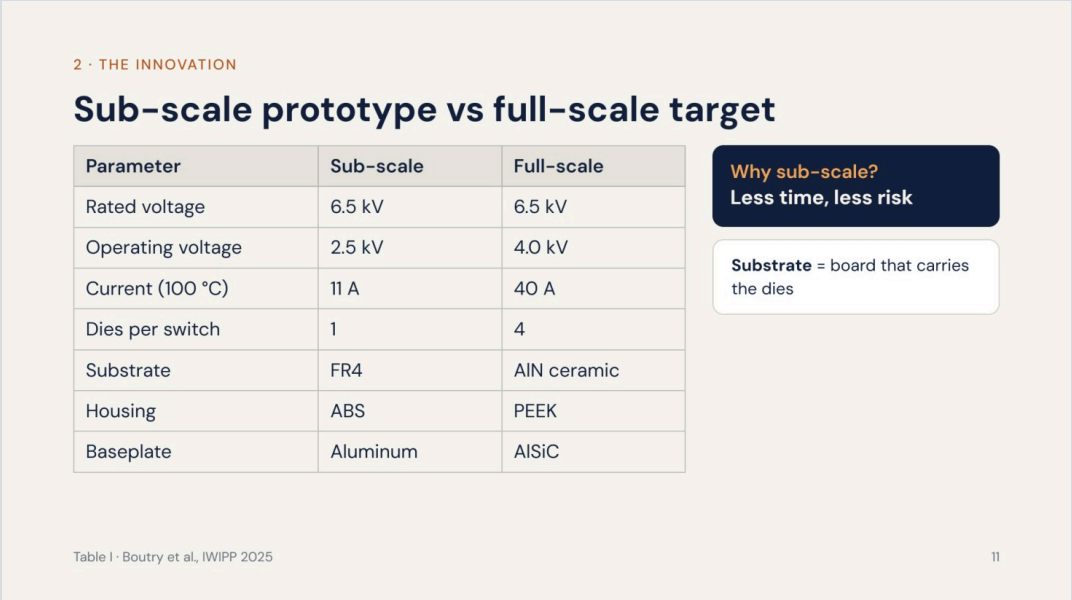


Figure 4. Sub-scale prototype versus full-scale target (data from the paper's Table I, own layout).

The sub-scale prototype trades performance for development time and risk: one die per switch instead of four, FR4 instead of an aluminium-nitride ceramic substrate, a 3D-printed ABS housing instead of PEEK, and an aluminium baseplate instead of AlSiC metal-matrix composite.

3 · How the prototype is built

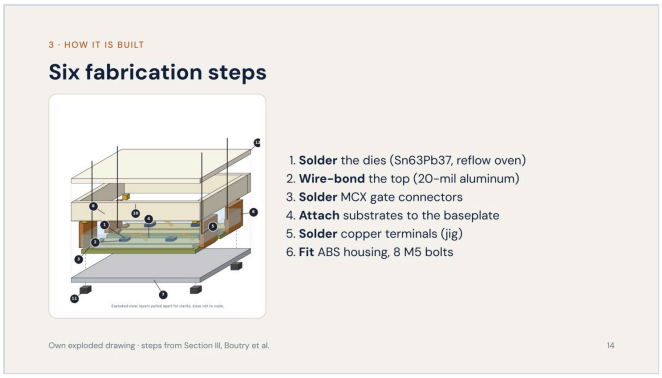


Figure 5. The six fabrication steps (own exploded drawing; steps from Section III of the paper).

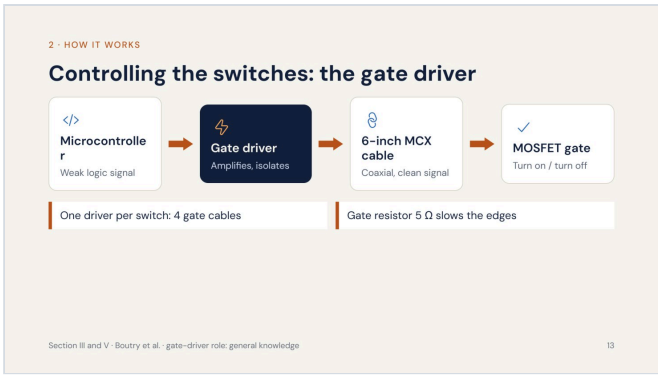


Figure 6. Gate path: controller → gate driver → 6-inch MCX cable → gate, with a 5 Ω gate resistor (own diagram).

1. **Die attach.** The dies are soldered to the substrate in a reflow oven with eutectic Sn63Pb37 solder, which melts at 183 °C. The drain, on the underside of the die, sits on this solder, so the joint carries both the drain current and the heat.
2. **Top-side interconnects.** 20-mil (0.5 mm) aluminium wires are ultrasonically bonded to source and gate pads, several in parallel.
3. **Gate connections.** MCX coaxial connectors are soldered directly to the substrates and linked to the gate drivers by 6-inch MCX cables. Coaxial cable keeps the gate loop small and clean. The connectors and cable ends are buried in silicone gel.
4. **Baseplate.** The finished substrates are attached to the baseplate.
5. **Power terminals.** Terminals machined from 0.04-inch (1 mm) copper are soldered while an aluminium jig, shaped like the end of the housing, holds them in place.
6. **Housing.** A 3D-printed ABS housing is fixed with eight M5 bolts threaded into pressed-in brass inserts.

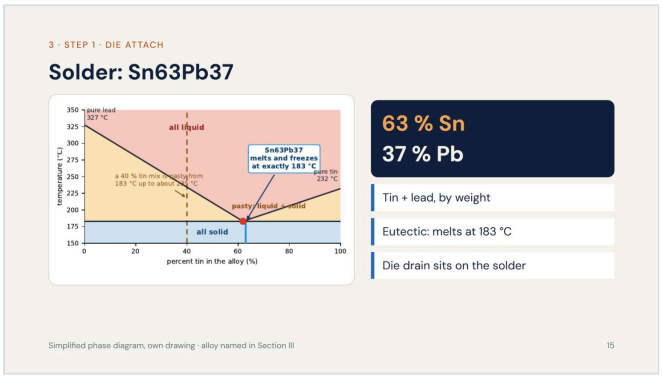


Figure 7. Simplified Sn–Pb phase diagram: the 63/37 eutectic melts at a single temperature, 183 °C (own drawing).



Figure 8. A typical reflow profile: preheat, soak, reflow above 183 °C, cool. The paper gives no profile; this is illustrative (own drawing).



Figure 9. Wire bonding with 20-mil aluminium wire (own drawing; wire size from the paper).

4 · Static characterization: parasitics and conduction

4.1 Parasitic inductance (ANSYS Q3D)

Before testing, the authors simulated the module's parasitics in ANSYS Q3D. To speed up the analysis, the bond wires were replaced by copper straps, a simplification the authors had validated before. A copper block shorted AC1 and AC2 so that the module could be analysed as one half bridge.

The key figure of merit is the **commutation inductance**, from DC+ to DC−: the inductance of the loop that the current must change in at every switching event. The simulated value is **34.5 nH**, above the 20 nH target for medium-voltage modules (Roll2Rail traction specification). The two DC-to-phase partial inductances are 45 and 46 nH, so the two legs are well balanced. All curves show two plateaus with a transition in the low-MHz range, explained by skin and proximity effects. The authors suggest that more overlap between the DC+ and DC− terminals would lower the inductance through flux cancellation.

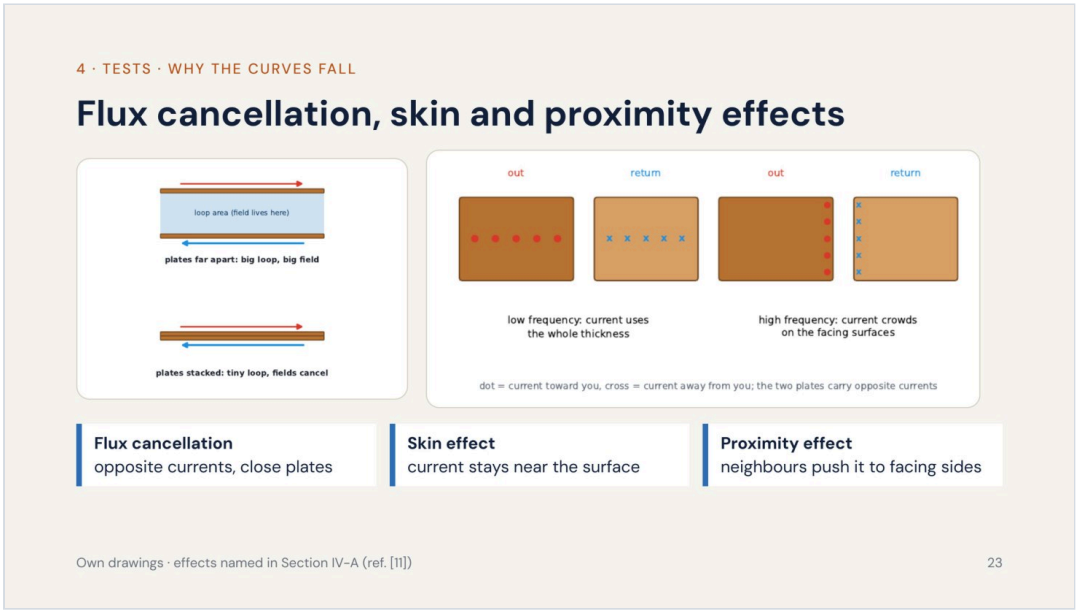


Figure 10. Why inductance falls with frequency: flux cancellation between close, opposite currents, and skin and proximity effects pushing current to the facing surfaces (own drawings).

4.2 Blocking and conduction (Keysight B1505A)

A B1505A curve tracer measured the leakage current up to **3.0 kV**, and the forward and third-quadrant (reverse) conduction up to **20 A**. The curves match the manufacturer's datasheet, including an on-resistance of about **300 mΩ** at room temperature. This shows that die attach and wire bonding did not degrade the dies.

5 · Dynamic characterization: the double-pulse test

For switching tests, AC1 and AC2 were joined with external busbars to make a half bridge. The University of Alabama medium-voltage double-pulse testbed uses a 7.5 kV dc-link capacitor bank and a low-capacitance, multi-element load inductor set to **4 mH**. Drain current was measured with a 2.5 mΩ coaxial shunt, drain-source voltages with 6 kV Tektronix differential probes, and gate-source voltages with optically isolated IsoVu probes.

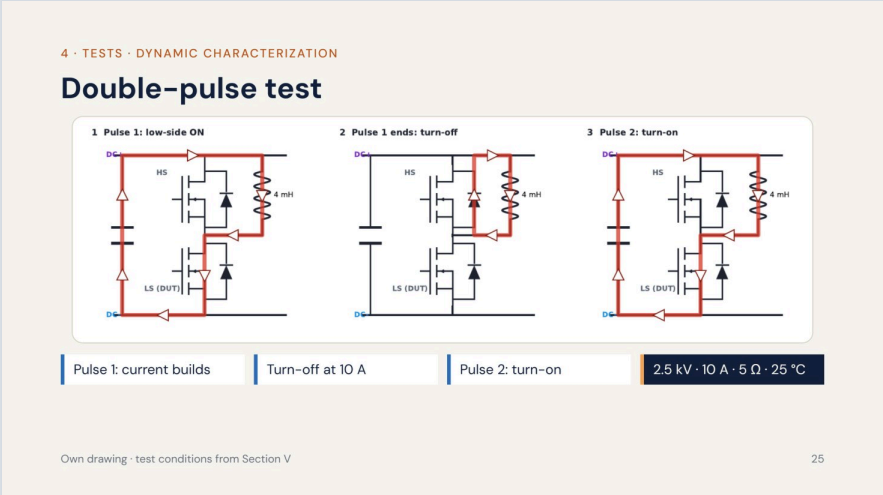


Figure 11. Double-pulse principle: the first pulse builds the load current, its end is the turn-off event, and the second pulse gives the turn-on event at the same current (own drawing; conditions from Section V).

Tests ran up to **2.5 kV and 10 A**, with a 5 Ω gate resistance, at 25 °C. With the 4 mH inductor, reaching 10 A at 2.5 kV takes only t = L·I/V = 4 mH × 10 A / 2.5 kV = 16 µs, so a short first pulse is enough. The results:

- **Turn-off overvoltage below 200 V**, modest despite the high commutation inductance.
- **Strong current ringing** at both turn-on and turn-off. My reading of the turn-on plot gives a peak near 44 A against a 10 A load. The authors note that the shunt's low resolution at these currents may contribute, but that measurement error does not explain all of it, since their earlier tests on the same dies showed similar waveforms.

The authors conclude that the concept is viable. Their future work is a full-scale prototype tested over a wider range of voltage, current and case temperature, plus dielectric ruggedness and partial-discharge testing.

6 · My analysis: what the results do and do not show MY ANALYSIS

The numbers below are my own first-order estimates from values in the paper and standard formulas. They are meant to frame questions, not to replace measurements.

6.1 What the 200 V overshoot says about switching speed

To first order, the turn-off overshoot is set by the commutation inductance and the rate of current fall:

$$\Delta V \approx L_\sigma \cdot |di/dt| \tag{1}$$

With L_σ = 34.5 nH and ΔV < 200 V, the turn-off di/dt must have stayed below about **5.8 A/ns**. At only 10 A that is plausible, since the current transition lasts a few nanoseconds. The low overshoot therefore does not mean the inductance is harmless. It means the test did not yet push the module hard. At the full-scale target of 40 A with a faster gate drive, the same inductance gives much more:

di/dt	1 A/ns	2 A/ns	5 A/ns	10 A/ns
ΔV with 34.5 nH (prototype)	35 V	69 V	173 V	345 V
ΔV with 20 nH (target)	20 V	40 V	100 V	200 V

On a 4.0 kV operating bus, 345 V of overshoot still leaves margin to 6.5 kV. The bigger cost is the energy stored in the loop and released as ringing and EMI, which grows with $L \cdot I^2$.

6.2 The current ringing is an EMI question

The ringing is a resonance between the loop inductance and the device and circuit capacitances, at $f_r \approx 1/(2\pi\sqrt{(L_\sigma \cdot C_{eq})})$. It is weakly damped because the loop resistance is small. Beyond measurement quality, a 44 A peak on a 10 A load matters for three reasons: it stresses the device, it radiates and conducts EMI in the tens-of-MHz range, and in a full bridge it can couple into the gate loops of the other leg. The paper does not report EMI measurements. I think it is the most important open point for a module meant for chargers and grid interfaces, which face strict emission standards.

6.3 Solder temperature margin

The die is rated for a 175 °C junction temperature, but the die-attach solder melts at 183 °C. Solder creep and fatigue depend on the homologous temperature T/T_m (in kelvin): at 175 °C, Sn63Pb37 runs at 448/456 = **0.98** of its melting point, and still 0.93 at 150 °C. Solder joints above about 0.5 T_m already creep significantly. The prototype can therefore not use the die's thermal rating. Power cycling would fatigue the joint long before the die. For the full-scale module, a higher-melting die attach such as sintered silver would be needed. Lead also raises the environmental issue in Section 8.

6.4 Test envelope versus rating

Quantity	Tested	Rated / target	Fraction
Leakage (blocking)	3.0 kV	6.5 kV	46 %
Switching voltage	2.5 kV	4.0 kV (full-scale operating)	63 %
Switching current	10 A	40 A (full-scale)	25 %
Temperature	25 °C	up to 175 °C junction	room temperature only

The full-scale operating point (4.0 kV on 6.5 kV devices, 62 %) follows usual practice for high-voltage SiC, where long-term failure rates from cosmic radiation rise steeply with DC-link voltage. Partial discharge, the main insulation risk at medium voltage, was not tested. FR4 and ABS are not suited to long-term operation at these field strengths and temperatures. The authors say so themselves, since the full-scale design moves to AlN, PEEK and AlSiC.

6.5 Conduction loss at full scale

With four 300 mΩ dies in parallel, each switch has about 75 mΩ at room temperature. At 40 A this gives $P = I^2R \approx 40^2 \times 0.075 =$ **120 W per conducting switch**, before switching losses. SiC MOSFET resistance rises with temperature (often by 1.5–2× towards 150–175 °C), so the hot value is higher. Moving from FR4 (about 0.3 W/m·K) to AlN ceramic (about 170 W/m·K) is therefore not optional at full scale.

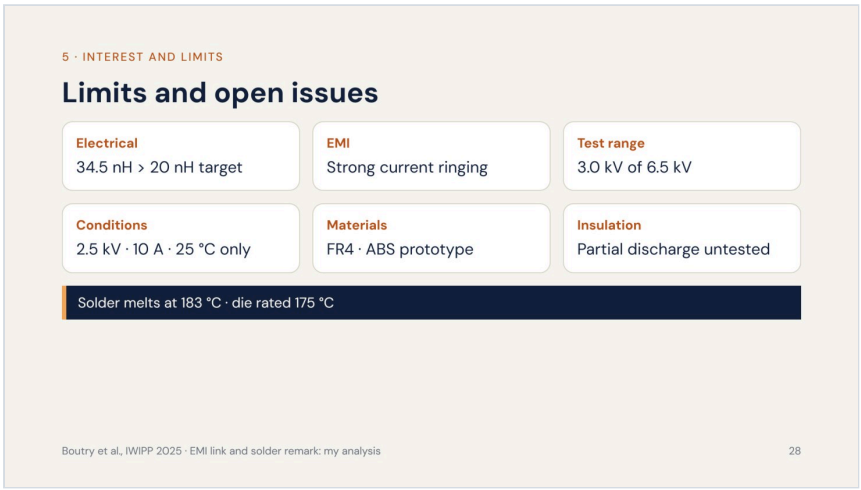


Figure 12. Summary of limits and open issues (own slide; the EMI and solder remarks are my analysis).

7 · Proposed simulation work PLANNED

The following is a plan I intend to carry out, not completed work. The goal is to make the analysis in Section 6 quantitative with tools I can access.

1. **Double-pulse model in LTspice.** Half bridge with the G2R300MT6 SPICE model if the manufacturer provides one (otherwise a behavioural model fitted to the datasheet), a 4 mH load, the 5 Ω gate resistance, and the commutation inductance as a lumped element. Calibrate against the paper's reported operating point (2.5 kV, 10 A, overshoot below 200 V).
2. **Inductance sweep.** Compare 34.5 nH with the 20 nH target at 10 A and 40 A: overshoot, ringing frequency, ringing amplitude and switching energy.
3. **Gate-resistance trade-off.** Sweep R_g from 5 to 20 Ω to see how much ringing a slower gate removes and what it costs in switching loss.
4. **Damping options.** Test an RC snubber across the DC link and a small damping resistance in the loop, and compare peak current and losses.
5. **Busbar overlap (stretch goal).** A simple 2D/3D estimate of how DC+/DC− overlap changes the loop inductance, to check the paper's suggested fix.

> Any results from this plan will be added to this report as a separate, dated section, with the model assumptions stated.

8 · Ethical, social and environmental aspects MY ANALYSIS



Figure 13. Issues beyond the lab (own analysis; not discussed in the paper).

- **Environmental.** Higher efficiency and faster EV charging are clear gains. On the other side, Sn63Pb37 contains lead, which RoHS restricts with exemptions for some high-temperature uses, and SiC wafer growth is energy-intensive.
- **Social.** Megawatt charging can speed up the electrification of heavy transport, but medium voltage brings safety and training requirements for installers and maintenance staff, and adds cost.
- **Ethical.** Reliability and honest reporting of limits matter when a module will run in vehicles and on the grid. The paper is clear about its sub-scale scope and future work, which I consider good practice.

9 · Conclusion

The paper shows that a 6.5 kV SiC full-bridge module in an XHP3 footprint can be built and switched, and its sub-scale prototype behaves as expected statically. Its main value is as a foundation: two symmetric half-bridge substrates in one standard package, with a clear path to the full-scale version. Reading it closely, the open questions are mostly packaging questions, not device questions: loop inductance and the ringing it causes, the thermal margin of the die attach, and insulation and partial discharge at medium voltage. These are the problems I would like to work on, starting with the simulations in Section 7.

References

[1] A. Boutry, M. Rogers, A. N. Lemmon, N. Turner and N. Baker, "A 6.5 kV Full-Bridge SiC MOSFET Module Design," 2025 IEEE International Workshop on Integrated Power Packaging (IWIPP), 2025, doi: 10.1109/IWIPP61784.2025.10971507.

[2] N. Baker, A. Lemmon and S. Jimenez Cardenas, "Characterization of 6.5 kV SiC MOSFETs with and without an Integrated On-Chip Schottky Diode," Proc. PCIM Europe, 2023 (cited in [1]).

[3] T. Wiik, "D1.2 New Generation Power Semiconductor: Common Specification for Traction…," Roll2Rail Consortium, 2016 (source of the 20 nH target, cited in [1]).

[4] S. Ramo, J. R. Whinnery and T. Van Duzer, *Fields and Waves in Communication Electronics*, 3rd ed., Wiley, 1997 (skin and proximity effects, cited in [1]).